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06EC45

Fourth Semester B.E. Degree Examination, December 2011
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the VHDL scalar data types. Compare the VHDL data types with verilog data types. **(08 Marks)**

b. If A, B and C are three unsigned variables with A = 11110000, B = 01011101, C = 00000000, find the value of
i) A NAND B ii) A && C iii) ~ | B iv) A ror 2 v) ! B vi) B << 1. **(06 Marks)**

c. Mention the different styles of writing the description using HDL. Explain the switch level and mixed type description by taking example. **(06 Marks)**

2 a. Explain with an example how the execution of the signal assignment statement takes place in HDL. **(04 Marks)**

b. Write the truth table and derive the Boolean functions after minimization for a full adder with active low enable i.e., if enable is low the sum and carry are the usual outputs of the adder. Then write a dataflow description using VHDL and include a delay of 2 ns for any gate including XOR. **(06 Marks)**

c. Obtain the Boolean expressions for a 2-bit comparator. Write the dataflow description in VHDL and verilog. **(10 Marks)**

3 a. Write a VHDL code for D-latch using i) signal assignment statements ii) variable assignment statements. Distinguish between these two types of statements with the help of simulation waveforms. **(08 Marks)**

b. Explain the general format of various loop statements in HDL, with examples. **(08 Marks)**

c. Write a verilog code to implement a 3-bit binary counter, with active high synchronous clear using case statement. **(04 Marks)**

4 a. Explain with suitable examples, how binding is achieved in the VHDL between
i) Entity and Architecture ii) Entity and Component iii) Library and Module. **(06 Marks)**

b. Write a structural description using VHDL to implement a 2:1 multiplexer, with active low enable. **(10 Marks)**

c. Explain the use of i) Generic statement ii) Parameter iii) Generate statement. **(04 Marks)**

PART – B

5 a. Give the significance of procedure, task and function. Compare them. **(05 Marks)**

b. Write a task to multiply two signed numbers, using the Booth algorithm. Use this task to perform signed vector multiplication, d = a * b , where a is a row vector with three elements and b is a column vector with three elements. **(10 Marks)**

c. Write a VHDL code to read a file consisting of four ASCII characters. **(05 Marks)**

6 a. Write a VHDL code for finding the greatest element of an array. Build a package for an array and use it in the code. **(08 Marks)**

b. Explain the implementation of arrays in VHDL and verilog. **(06 Marks)**

c. Write a verilog description of a 32×8 SRAM with the function table as shown in the Table Q.6(c). **(06 Marks)**

CS	$R/\overline{WR}$	Memory function
0	X	Deselected
1	1	Read cycle
1	0	Write cycle

Table Q.6(c)

7 a. How do you invoke a verilog module from a VHDL module? Explain by considering the mixed language description of a full subtractor using two half subtractors. **(08 Marks)**

b. Write a VHDL code for a 1-bit full adder, using the structural description. Invoke this VHDL code in a verilog module to implement a 3-bit adder with zero flag. The zero flag is set if output of adder is zero otherwise it is set to 1. **(12 Marks)**

8 a. What is synthesis? Discuss some important facts related to synthesis. **(06 Marks)**

b. Explain the VHDL synthesis information extraction from entity when the input and outputs are declared as i) Bit ii) Std_logic_vector iii) Unsigned iv) User defined type. **(08 Marks)**

c. Write a behavioral code in VHDL/verilog for a 2 to 4 decoder with active low output. Show the gate level synthesis of the code. **(06 Marks)**

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